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Some observations on the switching and memory phenomena in ZnTe–Si

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The *I–V* characteristics of p-ZnTe films deposited on ψ-Si using different growth conditions have been studied. The devices fabricated at substrate temperatures above 473 K possess bistable impedance states: switching from high-to-low impedance occurs when ZnTe film is positive biased, while switching from low-to-high impedance state occurs when ZnTe film is negative biased. It is observed that zero-based capacitance, open circuit photovoltage and short circuit current density are increased when the device is switched to the low impedance state and revert to their initial values when switched back to the high-impedance state. It is believed that an electronic switching mechanism is responsible, most probably the filling and the emptying of traps in the wide band gap ZnTe films.

1. Introduction

Bistable switching with memory has been observed in a number of thin film heterosystem devices [1–8]. An important feature of such bistable devices are the two impedance states; if any one of the states is selected the device will remain in the same state for a number of weeks under zero-bias conditions, thus it exhibits a memory capability.

In the present study, it is observed that ZnTe films deposited on a silicon substrate i.e. p-ZnTe–n-Si system exhibits memory switching effect. The dark d.c. *I–V* characteristics, zero-bias capacitance, open-circuit photovoltage and short circuit current density have been measured for ZnTe films deposited on a silicon substrate under different growth conditions.

2. Experimental details

Mirror polished silicon wafers (2.3 Ω/□, ⟨1 1 1⟩) were chemically cleaned by standard process [9] and immediately transferred to a deposition chamber of a vacuum coating unit. ZnTe films were grown on the substrate by thermal evaporation of pure ZnTe powder (99.998% Koch Light) in a vacuum of the order of 10^{-4} Pa. Rate of evaporation was kept constant at about 5 to 6 nm sec^{-1}. The thickness of the film grown varied from 50 to 300 nm and the substrate temperature was varied from room temperature to 613 K. Ohmic electrical contacts with the substrate were made by vacuum deposition of aluminium, while the contacts with the ZnTe film were made by vacuum deposition of gold (dot).

In the present studies, the perfect heterojunction between ZnTe and silicon is not formed. This may be due to

1. the fact that there is lattice mismatch between ZnTe and silicon of about 11.24%,
2. the possibility of formation of interface region and surface states between silicon and ZnTe films.

3. Results and discussion

The d.c. *I–V* characteristics were measured using a high impedance electrometer with suitable series resistance. Fig. 1 shows the characteristics obtained from the device fabricated at room temperature and having a film thickness about 150 nm. It is clearly seen that the current is an exponential function of the applied voltage in both the forward as well as reverse bias conditions. It has been observed that the device is permanently damaged or short-circuited when the bias exceeds 30 V, thus indicating that the switching effect is totally absent.

The absence of switching in ZnTe films deposited at room temperature may be attributed to the fact that these films were tellurium rich, i.e. non-stoichiometric [10], and had a low resistivity of the order of 10 Ω cm. This precludes the switching effect generally observed in tellurium-rich material [11].

The *I–V* characteristic of the system fabricated at a substrate temperature of 573 K and having a ZnTe film thickness about 150 nm is shown in Fig. 2. Switching takes place from the high impedance state A (i.e. OFF state) to the low impedance state B (i.e. ON state) in the forward biased region (ZnTe positively biased). This low impedance state B was maintained for about 25 days at zero bias and could be reproduced in the forward direction unless the device was biased in the reverse direction. In the reverse biased region, switching takes place from the low-impedance state C to the high impedance state D. This high impedance state is stable and the device remains in state D for an indefinite period with zero-biased conditions. Therefore, this phenomenon can be called the memory effect. The low impedance state (B–C), i.e. ON state, is nearly ohmic; whereas the high impedance state (A–D), i.e. OFF state, is non-linear and approximately symmetrical about the origin.

It can be seen that the memory becomes progressively shorter with the reverse bias along C (Fig. 2). It

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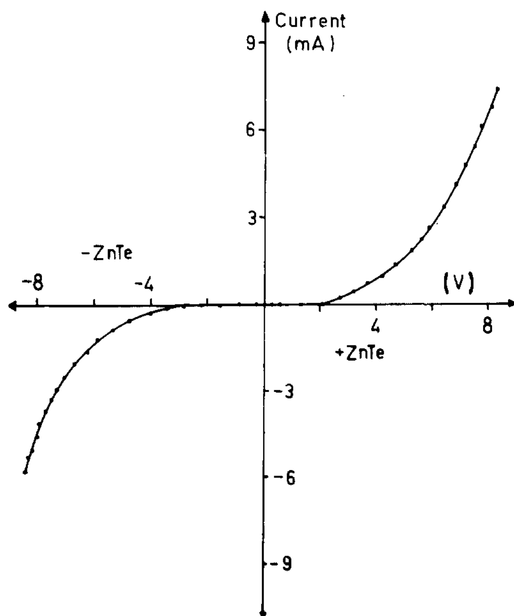

Figure 1 *I–V* characteristics of a p-ZnTe–n-Si device fabricated at room temperature.

lasts for about 20 days for currents as low as 0.1 to 0.2 mA and for about 20 h at 2.5 to 3.5 mA. When the threshold current exceeds 10 mA under the pulse condition the switching speed is about 10 nsec. A large number of switching cycles shows that the device follows the same switching path and has the same value of V_{th} and I_{th}.

ZnTe films deposited at substrate temperatures ranging from 473 to 613 K also show switching effects and have similar characteristics to those shown in Fig. 2. In this temperature range, the films possess a polycrystalline nature, a stoichiometric composition [10] and resistivity of the order of $10^7\,\Omega$cm. The symmetry nature of *I–V* characteristics in the high

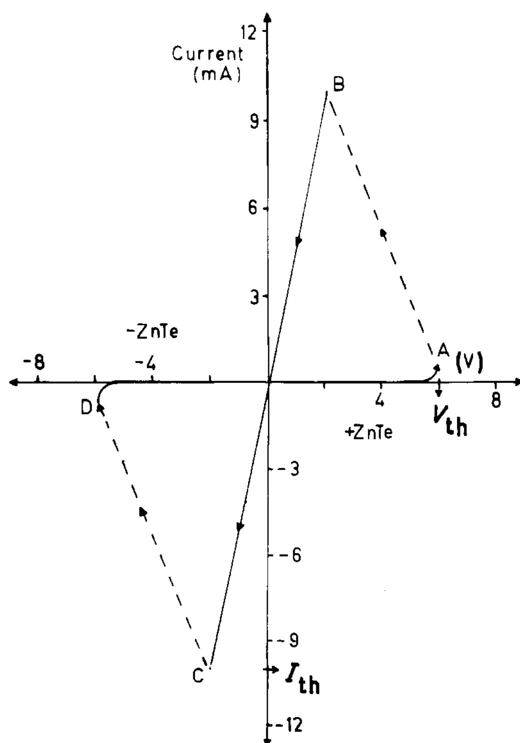

Figure 2 *I–V* characteristics of a p-ZnTe–n-Si device fabricated at 573 K.

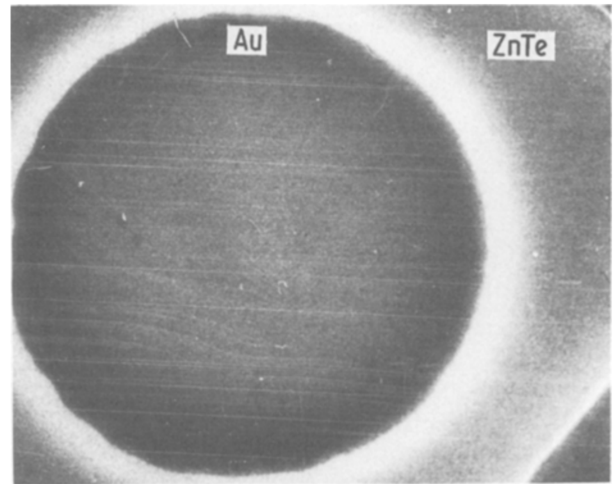

Figure 3 Backscattered electron micrographs of Au-ZnTe surface. (× 100).

impedance state about the origin indicates that the heterojunction is playing a minor role. The characteristic of the overall device is determined by the high resistivity ZnTe film. Hovel and Urgell [1, 2] have also reported that the high resistivity ZnSe layer plays a major role in switching mechanisms in ZnSe–Ge heterojunction. Okushi *et al.* [5] have obtained similar switching characteristics of the ZnTe–Si system but suggested that they are not essentially related to the polarized memory effect. The main reason for the phenomenon was due to damage appearing at Au–ZnTe interface.

In the present case, an optical microscope examination of the device surface did not reveal any morphological changes on the surface. The sample surface was also observed by scanning electron microscope for better resolution of any morphological changes. Fig. 3 shows a back scattered electron micrograph of the Au–ZnTe contact surface of the device (after removal of contact lead) after many repeating switching cycles. It is also revealed that the edge of the gold contacts remained intact. The formation of filaments, other morphological changes and damage are not observed on Au–ZnTe as well as on other parts of the device. Thus the behaviour of the switching device in the present case is considerably different from that reported by Okushi *et al.* [5].

It is believed that an electron switching mechanism is responsible, the most probable being the filling and the emptying of traps in the wide band gap and high resistivity ZnTe, which might take place preferentially at a stacking fault. The switching from A to B might be due to the trap filling by hole injection from the metal electrode. Traps being filled with holes, the high impedance state A would change into the low impedance state B. On the other hand, the switching from C to D might be due to the trap emptying. Traps filled with holes in state C would become empty with increase of the reverse bias and high impedance state D would occur, thus C–D switching takes place.

It appears that major requirements for obtaining this type of switching device are a thin semiconducting film containing a sufficient trap density and an interface region with a potential profile characteristic of a

TABLE I Characteristics of p-ZnTe–n-Si system (at constant ZnTe film thickness 150 nm)

Substrate temperature T_s (K)	Threshold voltage V_{th} (V)	Zero-bias capacitance C_0 (pF)		V_{oc}* (mV)		J_{sc}* (μA cm^{-2})	
		OFF state	ON state	OFF state	ON state	OFF state	ON state
473	6.2	2.7	14	95	180	132	205
573	6.0	1.5	17	125	345	120	340
613	6.8	2.7	17	116	250	95	180

*Measured at constant illumination of about 100 mW cm^{-2}.

Schottky barrier. Similar phenomena have been observed in ZnTe–InAs [4] and ZnSe–Ge [1, 2]. Traps in ZnTe film might be from some type of impurity band or shallow levels, working as sinks of conduction carriers. However, the exact confirmation requires a further detailed investigation.

Table I shows that open circuit photovoltage (V_{oc}), short circuit current density (J_{sc}) and zero-bias capacitance (C_0) are increased in the ON state. It is observed that V_{oc}, J_{sc} and C_0 revert to their initial values when the device is switched back to the OFF state. It is observed that threshold current I_{th} and threshold voltage V_{th} are independent of the intensity of illumination [12]. Therefore, the two impedance states are not influenced by photo-excitation during measurement of V_{oc} and J_{sc}. It is also observed that threshold voltage is independent of substrate temperature. However, it increases as the thickness of ZnTe film increases, indicating that a constant field strength of the order of about 10^6 V cm^{-1} is necessary for the switching transition.

4. Conclusions

In the p-ZnTe-n-Si system, the ZnTe film acts as semi-transparent electrode to the photon energy which gives the photovoltaic effect. When the device is switched to the ON state, due to filling of traps in ZnTe films, the zero-bias capacitance as well as open circuit photovoltage increases. However, the series resistance of the device decreases, which is ultimately responsible for the increase of short circuit current density. This clearly indicates that the device efficiency increases in ON state conditions.

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